Application No.: 09/853,005 7/10/03 Docket No.: JCLA5312

REMARKS

Present Status of the Application

In response to the Second Office Action dated March 13, 2003, Applicants respectfully request consideration of the following discussion on the rejection to the pending claims. No claims have been canceled, no claims have been added, and no claims have been amended. Accordingly, Claims 1-16 remain pending in the present application.

In the Second Office Action, the Examiner rejected Claims 1, 2, 4-6 under 35 U.S.C. §102(e) as being anticipated by Ziegler et al., USPN 6,182,176 (Ziegler). Furthermore, the Second Office Action rejected Claims 3, 7-9 under 35 U.S.C. §103(a) as being unpatentable over Ziegler. The Second Office Action also rejected Claims 10, 12 and 13 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of Handy "The Cache Memory Book" (Handy). The Examiner rejected Claim 11 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of "Handy", in further view of Islam et al., USPN 6,032,228 (Islam). The Office Action rejected Claims 14-16 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of Islam.

Concerning the Rejection of Claims 1, 2, and 4-6 Under 35 U.S.C. §102(e)

The Office Action rejected Claims 1, 2, 4-6 under 35 U.S.C. §102(e) as being anticipated by Ziegler et al., USPN 6,182,176 (Ziegler). Applicants have carefully reviewed the reference and respectfully traverse the rejection below.

Applicants respectfully submit that claim 1 patently defines over the cited prior art for at least the reasons stated in the response to the previous office action, and further in view of the reasons set forth as followed.

The Office Action restated that claim 1 is being anticipated by Ziegler because "a data buffer" is anticipated by the "element 166" of figure 2 and "peripheral device interface controller" is anticipated by the "controller which is a sub-element of the main memory controller 114" of figure 2 in the Ziegler.

Applicants do not agree with the assertions. The "element 166" of figure 2 in Ziegler is a **memory cache**. Regarding to the cache 166 of figure 2 in Ziegler, please refer to col.4, lines 33-39, as indicated by the Office Action, the **memory cache 166** is used for the **coherent transaction check**. As stated in col.4, lines 33-37, referred by the Office Action, each module that has a cache memory has a cache coherency queue for holding coherent transactions that have been issued on the bus until a cache coherency check can be performed", which is totally different from the "**data buffer**", as claimed in claim 1.

The asserted "controller which is a sub-element of the main memory controller 114" is not installed in neither the I/O Module 116 nor the processor 120. As shown in Fig.2 of the Ziegler, the controller is not installed in the neither the I/O Module 116 nor the processor 120, on

the contrary, the controller is installed in the "**main memory controller 114**", which used for determining the bus owner during the next available cycle. The I/O Module 116, as shown in Fig.2 of the Ziegler, has only a memory cache 166 and a Queue 162, no controller is introduced therein. Thus, the "peripheral device interface controller", which is ***installed within the control chip*** as claimed in claim 1, is not disclosed throughout the whole disclosures of the Ziegler.

Thus, the Ziegler does not disclose, either expressly or inherently described, a data buffer and a peripheral device interface controller ***installed within the control chip***, as addressed in claim 1.

On the contrary, the peripheral device interface control chip of the invention has a cache system including a buffer and a peripheral device interface controller. The peripheral device interface control chip having the cache system is capable of reducing latency period when data are read by a peripheral device. Furthermore, correctness of transmitted data is further ensured through a data synchronization method by the peripheral device interface control chip. The peripheral device interface control chip of the invention is used in the south bridge, which is not disclosed, either expressly or inherently described, by the Ziegler.

Thus, Ziegler does not anticipate claim 1, and the rejection should be withdrawn. If independent claim 1 is allowable over the prior art of record, then its dependent claims 2, 4-6 are allowable as a matter of law, because these dependent claims contain all features and elements of their respective independent claim 1.

The rejection of claims 1, 2 and 4-6, therefore, should be withdrawn.

Concerning the Rejection of Claims 3, 7-9 Under 35 U.S.C. §103(a)

The Examiner rejected Claims 3, 7-9 under 35 U.S.C. §103(a) as being unpatentable over Ziegler.

Incorporated reasons of independent claim 1 being distinguished over Ziegler set forth above, and also incorporated reasons set forth in the response to the previous office action, then its dependent claims 3, 7-9 are allowable as a matter of law, because these dependent claims contain all features and elements of their respective independent claim 1.

Concerning the Rejection of Claims 10, 12, and 13 under 35 U.S.C. §103(a) as being unpatentable over Ziegler, in view of Handy

The Office Action has rejected Claims 10, 12 and 13 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of Handy "The Cache Memory Book" (Handy).

In making the rejection, the Office Action correctly acknowledges that Ziegler neither discloses nor suggests a control chip includes a peripheral device interface controller and a data buffer and the central processing unit uses a MOESI protocol, and "modified state" and "exclusive state" for the cache data stream, as addressed in claim 10.

There is no requisite teaching, suggestion or motivation to combine the teachings of means of "MOESI protocol" in the Handy with the Ziegler to render claim 10 obvious to people of ordinary skill in the art. Furthermore, neither of the references applied against claim 10, along or in combination, shows or suggests that "when the cache data stream is in a modified state and if the data buffer executes a read operation from an address in memory that corresponds

to the cache data stream, the peripheral device interface controller inform the central processing unit to set the cache data stream into an owner state; and when the cache data stream is in an exclusive state and if the data buffer executes a read operation from the corresponding address, the peripheral device interface controller will inform the central processing unit to set the cache data stream into a shared state", as addressed in claim 10.

Incorporated reasons of independent claim 10 being distinguished over Ziegler in view of Handy set forth above, the claim 10 is allowable over the prior art of record, then its dependent claims 12 and 13 are allowable as a matter of law, because these dependent claims contain all features and elements of their respective independent claim 10.

Concerning the Rejection of Claim 11 under 35 U.S.C. §103(a) as being unpatentable over Ziegler, in view of Handy, in further view of Islam

The Office Action has rejected Claim 11 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of Handy, in further view of Islam et al. US Patent 6,032,228 (Islam).

Incorporated reasons of independent claim 10 being distinguished over Ziegler in view of Handy set forth above, the claim 10 is allowable over the prior art of record, then its dependent claim 11 is allowable as a matter of law, because these dependent claims contain all features and elements of their respective independent claim 10.

Concerning the Rejection of Claims 14-16 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of Islam

The Office Action has rejected Claims 14-16 under 35 U.S.C. §103(a) as being unpatentable over Ziegler in view of Islam.

In making the rejection, the Office Action correctly acknowledges that Ziegler neither discloses nor suggests most of the steps addressed in claim 14. The Office Action additionally relies on the teachings of Islam. However, Islam fails to disclose or otherwise suggest all of the state changes as addressed in claim 14, and also admitted in the Office Action on page 15, lines 5-8. Thus, this reference cannot possibly overcome the above-noted deficiencies of Ziegler. The Islam discloses a "Flexible cache-coherency mechanism." In the cache system, one or more cache components and a set of one or more consistency-replacement functions are provided. A cache component caches one or more items in its one or more cache entries. Items that hit in the cache can result in corresponding cache entries being read or written. There is no requisite teaching, suggestion or motivation to combine the teachings of means of "Flexible cache-coherency mechanism" in the Islam with the Ziegler to render claim 14 obvious to people of ordinary skill in the art.

Incorporated reasons of independent claim 14 being distinguished over Ziegler in view of Islam set forth above, the claim 14 is allowable over the prior art of record, then its dependent claims 15-16 are allowable as a matter of law, because these dependent claims contain all features and elements of their respective independent claim 14.

The rejection of claims 14-16, therefore, should be withdrawn.

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CONCLUSION

For at least the foregoing reasons, it is believe that all pending claims 1-16 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,
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